REMARKS

I. Introduction

In response to the pending Office Action, Applicants have cancelled claims 2 and 7 and amended claim 1 to further clarify the intended subject matter of the invention. Support for the amendments to claim 1 may be found in original claims 2 and 7 and on page 4, lines 15-17. In addition, claims 8-10 and 12 have been amended to show proper claim dependency. No new matter has been added.

In reviewing the file, it is noted that we have not received acknowledgement of the Information Disclosure Statement and cited art U.S. Patent No. 5,933,855 filed with the Application on July 23, 2003. Enclosed are copies of the Information Disclosure Statement, PTO-1449 and stamped return postcard acknowledgement. Applicants hereby respectfully request that the appropriately acknowledged PTO-1449 (re: US Patent No. 5,933,855) be furnished to Applicants and the record be clarified to confirm that the cited art has been considered and made of record.

For the reasons set forth below, Applicants respectfully submit that all pending claims are patentable over the cited prior art.

II. The Rejection Of Claims 2, 7-10 And 12 Under 35 U.S.C. § 102

Claims 2, 7-10 and 12 were rejected under 35 U.S.C. § 103(a) as being anticipated by Margulis (U.S. Pub. No. 2001/0040580) in view of Kosugi et al. (USP No. 6,640,019). As claim 1 has been amended to incorporate the limitations of claims 2 and 7, the § 102 rejection of claim 1 has been rendered moot and the § 103 rejections of claims 2 and 7 will be addressed as a § 103

rejection of claim 1. Applicants respectfully traverse the pending rejections of the above cited claims for at least the following reasons.

With regard to the present invention, amended claim 1 recites, in-part, a semiconductor integrated circuit device that operates while being connected to an external processing unit, comprising: a plurality of internal memories; a first processing unit for data processing and a second processing unit for data processing; a first data bus connected to the first processing unit; a second data bus connected to the second processing unit; a third data bus dedicated to the external processing unit; a first bus selector for selectively connecting the first processing unit with the first data bus or the second data bus; a second bus selector for selectively connecting the second processing unit with the first data bus or the second data bus; a first memory interface, mediating and controlling DMA data transfer requests from the first processing unit and second processing unit, which is interposed between the memory assigned to the first processing unit and the first data bus; a second memory interface, mediating and controlling DMA data transfer requests from the first processing unit and second processing unit, which is interposed between the memory assigned to the second processing unit and the second data bus.

The Examiner alleges that Fig. 5 of Margulis teaches each of the limitations of claim 1 of the present invention except a first bus selector for selectively connecting the first processing unit with the first data bus or the second data bus and a second bus selector for selectively connecting the second processing unit with the first data bus or the second data bus. The Examiner then alleges that Margulis teaches this limitation in Figs. 9 and 10. However, there is no suggestion that the embodiments disclosed in Fig. 9 or 10 **can** be combined with the embodiment disclosed in Fig. 5. However, in Fig. 5, there is no apparent way to connect the first processing unit 506 with the second data bus 536. The first processing unit 506 can only be

connected with the first data bus 534. Similarly, there is no apparent way to connect the second processing unit 508 with the first data bus 534. The second processing unit 508 can only be connected with the second data bus 536. Further, as Fig. 9 does not show a first data bus and second data bus, and Fig. 10 does not show a first and second processing unit, these embodiments do not cure the deficiencies of Fig. 5, nor do they appear to be combinable with the embodiment shown in Fig. 5. Hence, the proposed combination of Figs. 5, 9 and 10, which describes ***different*** embodiments of the invention in Margulis, is invalid. Therefore, Margulis does not teach or suggest all of the limitations of amended claim 1 of the present invention.

Turning to Kosugi, the Examiner alleges that Kosugi teaches that in an analogous system, at least first and second memory interfaces that handle DMA transfers between memories (see DMAC 107, 112, and 115 in Fig. 3 of Kosugi). However, there appears to be no mention in Kosugi of the first and second memory interfaces respectively *mediating and controlling* DMA data transfer requests from the first and second processing units. As can be seen in Fig. 1 of the present invention, and described on page 4 of the specification,

> The memory controller **30** further includes a work region memory interface (WMIF) **32** serving as a first memory interface, a frame region memory interface (FMIF) **33** serving as a second memory interface, and a CPU region memory interface (CPUIF) **34** serving as a third memory interface....The WMIF **32** is interposed between the work region assigned to the main processor **24** and the WM bus **40**, and mediates and controls DMA data transfer requests. The FMIF **33** is interposed between the frame region assigned to the video interface **25** and the graphics processor **26** on the one hand and the FM bus **41** on the other hand, and mediates and controls DMA data transfer requests. ...Thus, the

> memory assigned to the work region can be accessed via the WMIF **32**, the memory assigned to the frame region can be accessed via the FMIF **33**.

Kosugi fails to disclose a feature in which the first and second memory interfaces respectively mediate and control DMA data transfer requests from the first and second processing units as described in the passage recited above. Furthermore, assuming *arguendo* that Kosugi did disclose this feature, there appears to be no suggestion to combine Kosugi with Margulis. Accordingly, it appears that neither Margulis nor Kosugi teach claim 1 as currently amended.

In order to establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA1974). At a minimum, as both Margulis and Kosugi fail to teach or suggest a semiconductor integrated circuit device that operates while being connected to an external processing unit, comprising a first bus selector for selectively connecting the first processing unit with the first or the second data bus, a second bus selector for selectively connecting the second processing unit with the first or the second data bus, a first memory interface, mediating and controlling DMA data transfer requests from the first and second processing units, which is interposed between the memory assigned to the first processing unit and the first data bus, and a second memory interface, mediating and controlling DMA data transfer requests from the first and second processing units, it is submitted that Margulis and Kosugi, alone or in combination, do not render claim 1 obvious.

III. All Dependent Claims Are Allowable Because The Independent Claim From Which They Depend Is Allowable

Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claim 1 is patentable for the reasons set forth above, it is respectfully submitted that all pending dependent claims are also in condition for allowance.

IV. Conclusion

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication of which is respectfully solicited.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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Date: June 26, 2006

Applicant: Masayoshi TOJIMA, et al. Docket No. 60188-616

Title: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE Serial/Reg./Patent No. Not Yet Assigned

Date Sent: 7/23/2003 ☒ Hand Carried ☐ Fax ☐ Electronic ☐ Cert. of Mailing ☐ Express Mail No. _____

☒ Transmittal Letter

New Patent App ☒ Utility ☐ Design ☐ Cont. ☐ CIP ☐ Div. ☐ PCT ☐ RCE ☐ Prov

☐ Other: _____

11 pages of Specification
3 pages of Claims
1 pages of Abstract
7 pages of Formal Drawings
☐ Small Entity ☒ Large Entity
☒ Declaration/Power of Attorney
☒ Recordation of Assignment
☒ Information Disclosure Statement
1 Form PTO 1449
5 copies of cited references
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THE PATENT AND TRADEMARK OFFICE DATE STAMPED HEREON IS ACKNOWLEDGEMENT THAT THE ITEMS, CHECKED ABOVE, WERE RECEIVED BY THE PTO ON THE DATE STAMPED.

Docket No.: 60188-616

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of	:	
Masayoshi TOJIMA, et al.	:	
Serial No.:	:	Group Art Unit:
Filed: July 23, 2003	:	Examiner:

For: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

INFORMATION DISCLOSURE STATEMENT

Mail Stop Patent Application
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the documents listed on the attached form PTO-1449. It is respectfully requested that the documents be expressly considered during the prosecution of this application, and that the documents be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

This Information Disclosure Statement is being filed within three months of the U.S. filing date OR before the mailing date of a first Office Action on the merits. No certification or fee is required.

The relevance of each non-English language reference is discussed in the present specification.

Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,

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INFORMATION DISCLOSURE CITATION IN AN APPLICATION

(PTO-1449)

ATTY. DOCKET NO.	SERIAL NO.
60188-616	
APPLICANT: **Masayoshi TOJIMA, et al.**	
FILING DATE: **July 23, 2003**	GROUP

U.S. PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Document Number Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		US 5,933,855	08/03/1999	RUBINSTEIN	
		US			
		US			
		US			
		US			
		US			
		US			
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FOREIGN PATENT DOCUMENTS

EXAMINER'S INITIALS	CITE NO.	Foreign Patent Document Country Codes-Number-Kind Codes (if known)	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines Where Relevant Figures Appear	Translation Yes	Translation No
		JP 10-27131	01/27/1998	MATSUKAWA		abstract	
		JP 10-260952	09/29/1998	KAJITANI		abstract	
		JP 2000-99391	04/07/2000	OWADA		abstract	
		JP 2001-43180	02/16/2001	KURAFUJI, et al.		abstract	

OTHER ART (Including Author, Title, Date, Pertinent Pages, Etc.)

EXAMINER'S INITIALS	CITE NO.	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.

EXAMINER	DATE CONSIDERED
	3/13/06

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

1 Applicant's unique citation designation number (optional). 2 Applicant is to place a check mark here if English language Translation is attached.